9.2 A Current Driver IC using a S/H for QVGA Full-Color Active-Matrix Organic LED Mobile Displays

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There are three well-known methods for driving AMOLEDs: voltage driving, digital driving, and current driving schemes. Of these the current driving scheme is one of the most suitable solutions for AMOLEDs. It provides compensation for the Vth variation of the panel's TFTs, mobility and IR Drop, though it has a problem with respect to write time. In particular, the write time representing low gray data is too long. In order to represent a low portion of the grayscale, a minimum current level in the range of several nano-amperes needs to be obtained, which is very hard to program at the AMOLED panel during the line time. In a practical circuit design, the minimum current to be controlled should be approximately 10nA. This is very challenging because the transistor needs to be biased in the sub-threshold region where the threshold voltage variation effect is significant. A current driving design, based on a sample-and-hold (S/H) method, is developed to address this issue.

Figure 9.2.1 shows LTPS AMOLED pixel circuit and its control signal-timing diagram. This programming method is easy to implement and has a good current sampling performance, while the main limitation arises from the programming of the low gray level. The storage capacitor charging time will consume a large portion of the given line time, because low gray current level is just several nA. Moreover, the driving transistor may operate in the sub-threshold region. In order to solve these critical problems, we apply a boost technique using a sufficiently large current at the programming phase while boosting the gate voltage of the driving transistor by the boost capacitor (C_{boost})

The timing diagram for this IC is shown in Fig. 9.2.2. Four data values are latched on the falling edge of DCLK and sent to four DACs. The signals DCLK_1 to DCLK_4 and STPL_1 to STPL_4 are needed to generate the signals S/R_1 to S/R_4 to operate the Shift Registers for each DAC. So, each current DAC processes 180 data values for 60 X RGB channels. Four DACs are used instead of one common DAC to increase the settling time in the output channels. If only one DAC is used, the operating speed is too high for one output channel to settle within a dot clock. A four-DAC scheme provides for sufficient time margin, though it may be possible to decrease the number of DACs further.

Figure 9.2.3 shows the output circuit and one channel block diagram in the driver IC. The output channel scheme adopts a current-sink-type switched current memory cell [3]. Its output current level can be fully controlled from 10nA to 10uA. In the S/H scheme, there exists the central common DAC and the copier circuit in the output channels instead of the conventional channel DAC. The copier circuit must exactly duplicate the current from the common DAC. To this purpose, a matrix-type 8b segmented current DAC and the current-mirror type copier circuit is applied. The S/H function is performed in the copier circuit. That is, the gate-source voltage of MN1 corresponding to the D/A converted current is sampled by switch S1 and S2 and held at the capacitor C_{st}. During S/H, capacitor coupling, channel length modulation, charge injection, and clock feed-through may occur. So, to reduce the capacitor coupling, we use a Cascode-type current mirror to prevent channel-length modulation. We also select the length of MN1 to be very large because of mismatch characteristics of MN1. And, we use transmission gate switches in combination with dummy switches to decrease charge injection effects.

During one line interval time, the current DAC should copy current corresponding to the image data to all output channels. This means that one pixel write data must be copied to the output current memory cell in one dot clock. Thus, the DAC should supply the current to all output channels at high-speed relative to conventional schemes. In order to realize high-speed operation, a high-speed decoding circuit and a fast settling current source have been developed. The DAC consists of a 4b thermometer DAC and a 4b binary weighted DAC [4]. Figure 9.2.4 shows the architecture of a segmented DAC and switching sequence matrix. Current source, current switches and the local decoder have been optimally designed with respect to output settling time. The output settling time of the DAC is about 15ns. The good matching characteristic and high accuracy of the DAC has been achieved by adopting a current-cell matrix configuration and symmetrical switching sequence.

Color extension from 26k to 16M color is realized using a LUT. The gamma characteristic of OLEDs do not follow a linear function in very low luminance condition or very high luminance condition. Thus, we rely on the LUT scheme to compensate for abnormal gamma curves, thus 18b image data is converted to 24b image data.

Figure 9.2.5 and 9.2.6 shows measured results of this driver. Figure 9.2.5 is the deviations of the 5 channels from the left end to the right end channel with 4 different gray scales 63-, 31-, 15- and 7-gray shown in graphic form. The maximum output deviation is under 2%, which meets the target specification. Figure 9.2.6 shows the output current linearity of the 64 gray-scale.

Figure 9.2.7 shows a micrograph of the driver layout. The driver IC was fabricated in a 0.18μm 2P4M 5.5V high voltage CMOS process. Block A contains 720 S/H output channels. Block B contains the Controller. Block C contains 8b DACs and Block D contains the bias block. The total chip size was 19260×1780um^2 including test circuits.

To summarize, a sink-type current driver IC has been developed with 720 outputs, 64 gray levels (internal 256 gray levels), and a 10nA to 10μA controllable current range for LTPS QVGA full-color AMOLED displays. This driver is uses a sample-and-hold method controlling a small current range. This scheme reduces the output channel size by 30% compared to the conventional current driver scheme and reduces current level deviation per channel, thus finding application to high resolution and the high color depth AMOLED displays.

References:

[1] I. O'Conner, A. Kaiser, "Automated Synthesis of Current-Memory Cells," *IEEE Trans. Computer-Aided Design*, vol. 19, no. 4, pp. 413-424, April, 2000.
[2] C. Wang, M. Omair Ahmad and M.N.S. Swamy, "Design of a Transistor Mismatch Insensitive Switched Current Memory Cell," *IEEE Trans. Circuits and Systems*, vol. 2, no. 6, pp. 105-108, June, 1999.
[3] W. Guggenbuhl, J. Di, et al., "Switched-Current Memory Circuits for High-Precision Applications," *IEEE J. Solid-State Circuits*, vol. 29, no. 9, pp. 1108-1116, Sept., 1994.
[4] T. Miki, et al., "An 80-MHz 8-bit CMOS D/A Converter," *IEEE J. Solid-State Circuits*, vol. 21, no. 12, pp. 983-988, Dec., 1986.

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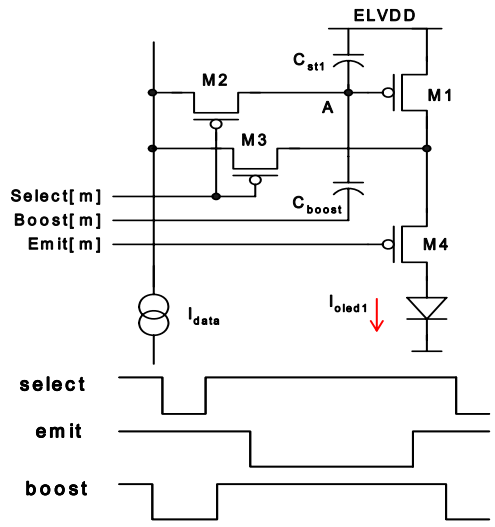

Figure 9.2.1: LTPS AMOLED pixel circuit.

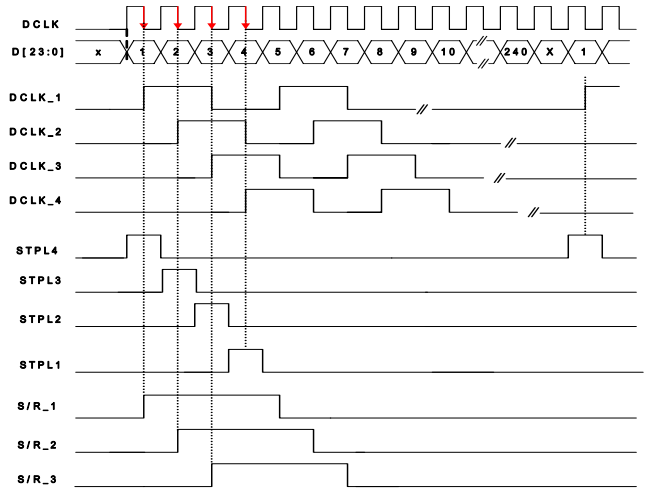

Figure 9.2.2: Timing diagram.

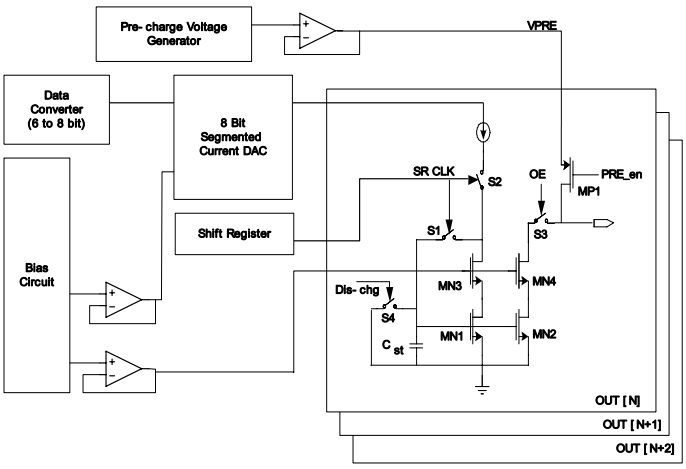

Figure 9.2.3: Sample-and-hold driving structure.

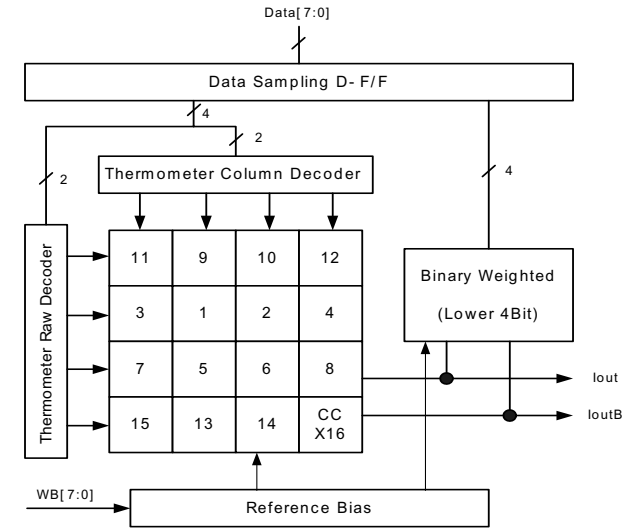

Figure 9.2.4: 8b segmented DAC structure.

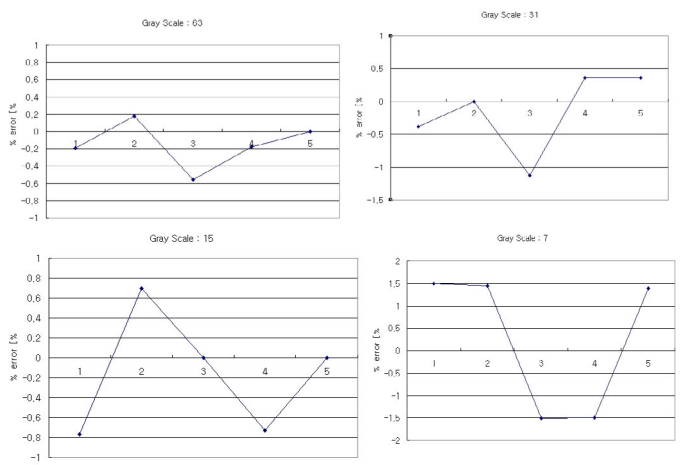

Figure 9.2.5: DIPP (Pin to Pin deviation of output current) at the grayscale-63/31/15/7.

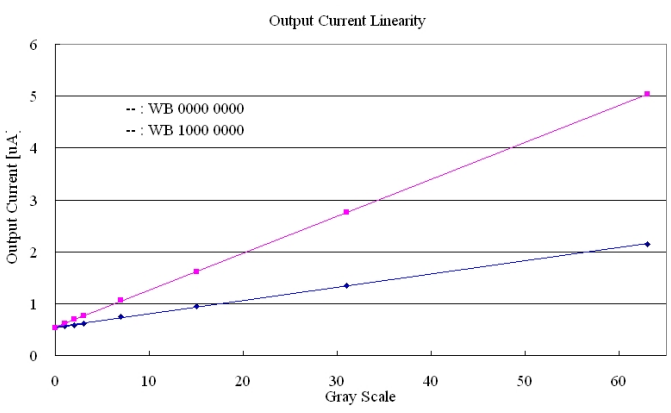

Figure 9.2.6: Driver output current linearity.

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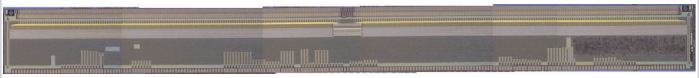

Figure 9.2.7: Die micrograph.

